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(54) **METHODS FOR MANUFACTURING SEMICONDUCTOR DEVICES HAVING CHAMFERED METAL SILICIDE LAYERS**

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(57) **ABSTRACT**

Methods for manufacturing a semiconductor device, in which a chamfered metal silicide layer is formed by a 2-stage continuous wet etching process using different etchants, thereby resulting in a sufficient insulation margin between a lower conductive layer including the metal silicide layer and the contact plug self-aligned with the lower conductive layer are disclosed. In the manufacture of a semiconductor device, a mask pattern is formed on a metal silicide layer to expose a portion of the metal silicide layer. The exposed portion of the metal silicide layer is isotropically etched in a first etchant to form a metal silicide layer with a shallow groove, and defects due to the silicon remaining on the surface of the metal silicide layer with the shallow groove are removed using a second etchant, to form a metal silicide layer with a smooth surface. Microelectronic structures produced by methods of the present invention are also disclosed.

17 Claims, 6 Drawing Sheets